What is claimed is:

1. A method of forming a thick metal silicide layer on a gate electrode, the method comprising:

forming a gate electrode of a transistor on a semiconductor substrate, wherein a hard mask is formed on the gate electrode;

forming a spacer on a sidewall of the gate electrode;

forming a first silicide layer on a portion of the semiconductor substrate, adjacent to the spacer;

forming an insulating layer on the first silicide layer to expose upper portions of the hard mask and the spacer;

selectively etching the exposed upper portions of the hard mask and the spacer using the insulating layer as an etch mask until the top surface and the sidewall of the gate electrode are exposed;

forming a metal layer on the exposed top surface and sidewall of the gate electrode; and

forming a second silicide layer on the gate electrode by siliciding the metal layer.

2. The method of claim 1, wherein the insulating layer is formed of a material having an etch selectivity with respect to the hard mask and the spacer.

3. The method of claim 2, wherein the hard mask is formed of a silicon nitride.

4. The method of claim 2, wherein the spacer is formed of a silicon nitride.

5. The method of claim 2, wherein the insulating layer is formed of a silicon oxide.

6. The method of claim 1, wherein forming the insulating layer comprises:

depositing the insulating layer on the first silicide layer; and

planarizing the insulating layer so as to expose the top surface of the hard mask and the upper portion of the spacer.

7. The method of claim 6, wherein planarizing the insulating layer comprises:

planarizing the insulating layer using the top surface of the hard mask as an etch stop point; and

detecting the etch stop point and further performing the planarization.

8. The method of claim 6, wherein planarizing the insulating layer is performed using chemical mechanical polishing.

9. The method of claim 1, wherein the second silicide layer is formed of a different material from the first silicide layer.

10. The method of claim 9, wherein the first silicide layer is formed of a cobalt silicide layer, and the second silicide layer is formed of a nickel silicide layer.

11. The method of claim 1, wherein the second silicide layer is formed to be thicker than the first silicide layer according to the width of a contact region between the sidewall of the gate electrode and the metal layer.

12. A method of forming a thick metal silicide layer on a gate electrode, the method comprising:

forming a gate electrode of a transistor on a semiconductor substrate, wherein a hard mask is formed on the gate electrode;

forming a spacer on the sidewall of the gate electrode;

forming a first silicide layer on a portion of the semiconductor substrate, adjacent to the spacer;

forming an etch stop layer on the first silicide layer to be extended so as to cover the hard mask and the spacer;

forming an insulating layer on the etch stop layer to selectively expose a portion of the etch stop layer that overlaps upper portions of the hard mask and the spacer;

selectively etching the exposed portion of the etch stop layer and the upper portions of the hard mask and the spacer disposed under the etch stop layer until the top surface and the sidewall of the gate electrode are exposed;

forming a metal layer on the exposed top surface and sidewall of the gate electrode; and

forming a second silicide layer on the gate electrode by siliciding the metal layer.

13. The method of claim 12, wherein the insulating layer is formed of an insulating material having an etch selectivity with respect to the etch stop layer, the hard mask, and the spacer.

14. The method of claim 13, wherein the etch stop layer, the hard mask, and the spacer are formed of silicon nitrides.

15. The method of claim 13, wherein the insulating layer is formed of a silicon oxide.

16. The method of claim 12, wherein forming the insulating layer comprises:

depositing the insulating layer on the etch stop layer; and

planarizing the insulating layer such that a shoulder portion of the etch stop layer is exposed.

17. The method of claim 16, wherein planarizing the insulating layer comprises:

planarizing the insulating layer using the top surface of the etch stop layer as an etch stop point; and

detecting the etch stop point and further performing the planarization until the lateral shoulder portion of the etch stop layer is exposed.

18. The method of claim 12, wherein the second silicide layer is formed of a different material from the first silicide layer.

19. The method of claim 18, wherein the first silicide layer is formed of a cobalt silicide layer, and the second silicide layer is formed of a nickel silicide layer.

20. The method of claim 12, wherein the second silicide layer is formed to be thicker than the first silicide layer according to the width of a contact region between the sidewall of the gate electrode and the metal layer.